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2 Introduction

Zefant XS3 is a tiny Spartan-3 based module containing all components required for a complete and powerful FPGA platform. It is projected to provide a reusable plug&play solution, enabling the user to focus on the basics of his project.

3 Quick Start

3.1 Checklist before PowerUp

3.1.1 *Settings on Zefant module*

- SB1301 MUST be set if no external voltage is provided for banks 2/3
- SB1301 MUST NOT be set if an external voltage is provided for banks 2/3
- JTAG DIP-Switches C/D of SW1201 must be set according to chapter 4.7.2
- SB1401 MUST be set if you want to use JTAG port on TopDown baseboard. See 4.7.3 for more informations. In case of a module stack, this applies only to the bottom-most module.
- SB1401 MUST NOT be set on any other module than the bottom-most of stack, a short circuit between the 3.3V rails of neighbour modules would be caused.

3.1.2 *Settings on TopDown baseboard*

- SB201/SB202 MUST be set to enable the power supply of the Zefant module

4 Hardware Description

4.1 PCB top view

Red: Component IDs
Blue: Pin Numbers

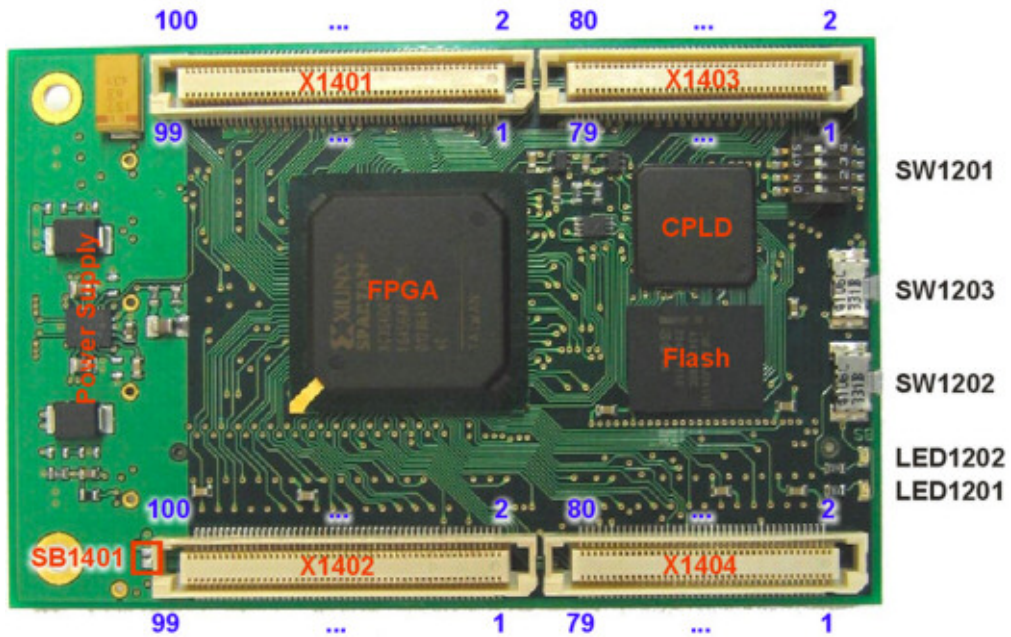


Fig. 4-1: Top side of Zefant FPGA module

4.2 PCB bottom view

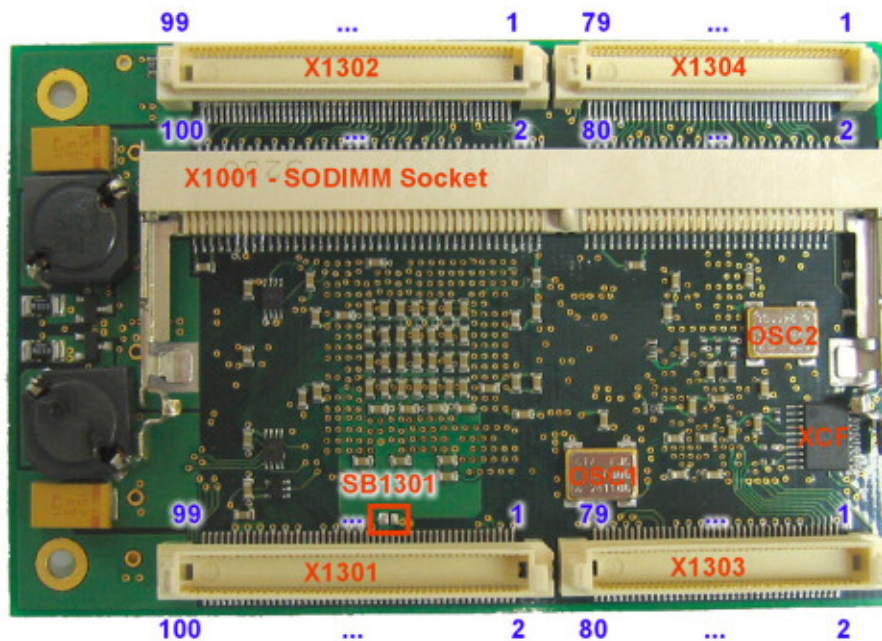


Fig. 4-2: Bottom side of Zefant FPGA module

4.3 Mechanical Dimensions

A baseboard compatible with the Zefant module contains 4 Hirose FX8C connectors. They have to be placed as shown below. The following drawings are available as Protel PCB files and Gerber data on the website for your reference.

4.3.1 "TopDown" Mounting

To mount a Zefant module with the FPGA side pointing to the baseboard, 2 FX8C-80P and 2 FX8C-100P connectors are placed on the baseboard as shown here:

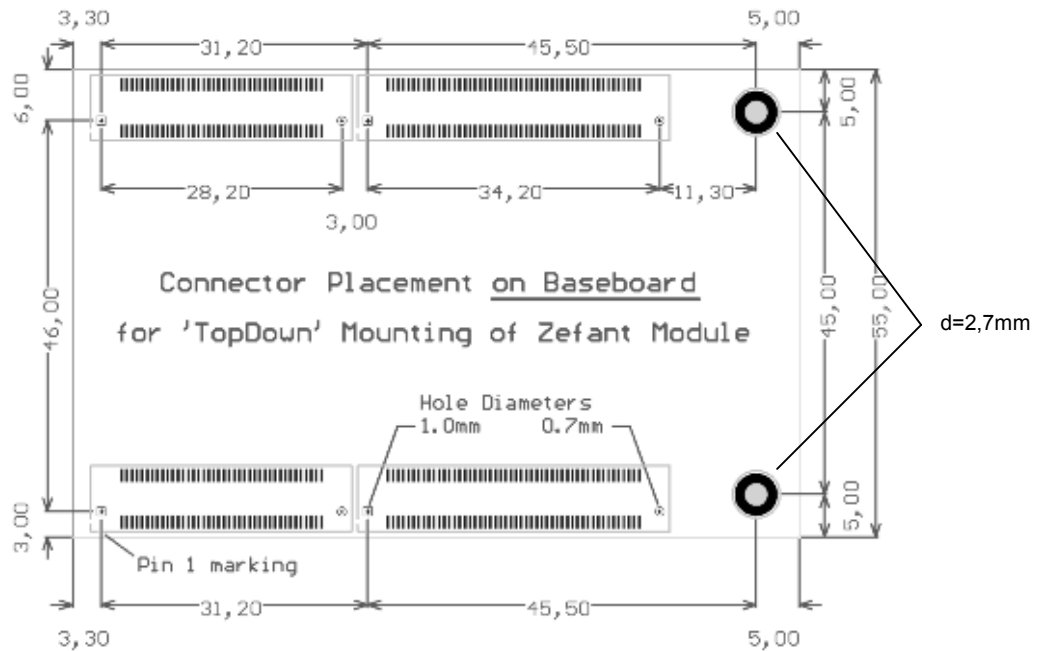


Fig. 4-3

4.3.2 "TopUp" Mounting

To mount a Zefant module with the SODIMM side pointing to the baseboard, 2 FX8C-80S and 2 FX8C-100S connectors are placed on the baseboard as shown here:

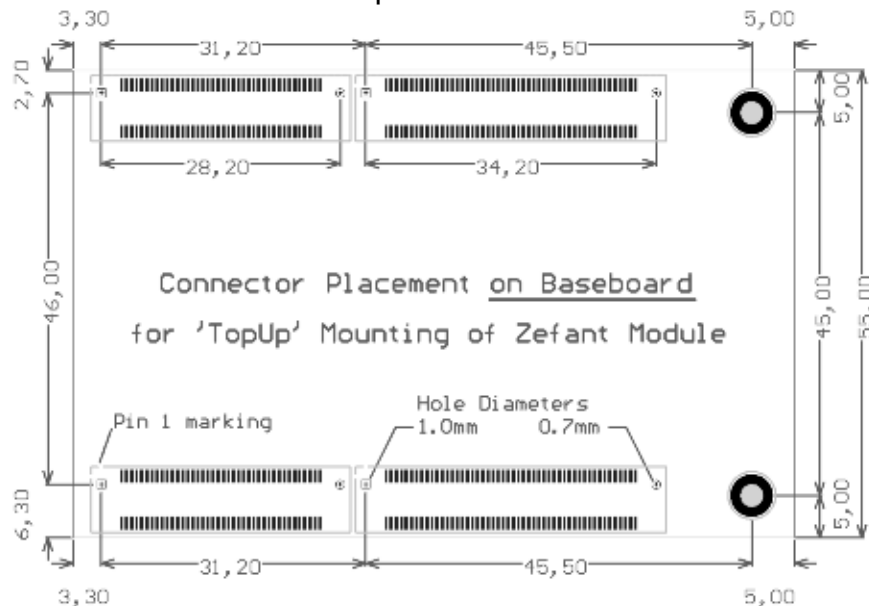


Fig. 4-4

4.4 Connectors

There are four Hirose FX8C board-to-board connectors on each side of the FPGA module:

Connector	Module side	Part Number	Digikey Order Number
X1401 X1402	Top (FPGA side)	FX8C-100S-SV(21)	H1248-ND
X1403 X1404	Top (FPGA side)	FX8C-80S-SV(21)	H1247-ND
X1301 X1302	Bottom (SODIMM side)	FX8C-100P-SV4(21)	H1236-ND
X1303 X1304	Bottom (SODIMM side)	FX8C-80P-SV4(21)	H1232-ND

Please note, that these part numbers will change during 2006 due to ROHS compatibility.

4.5 Mating connectors

Depending on the selection of the mating connectors, different stacking heights can be achieved.

4.5.1 Mating connectors for Top/FPGA side

Mates with	Resulting stacking height	Hirose Part Number	Digikey Order Number	Simple Solutions Order Number
X1401 X1402	5mm	FX8C-100P-SV(21)	H1223-ND	FX8C-100P
	6mm	FX8C-100P-SV1(21)	H1234-ND	
	7mm	FX8C-100P-SV2(21)	H1235-ND	
	9mm	FX8C-100P-SV4(21)	H1236-ND	FX8C-100P4
	11mm	FX8C-100P-SV6(21)	H1237-ND	
X1403 X1404	5mm	FX8C-80P-SV(21)	H1222-ND	FX8C-80P
	6mm	FX8C-80P-SV1(21)	H1230-ND	
	7mm	FX8C-80P-SV2(21)	H1231-ND	
	9mm	FX8C-80P-SV4(21)	H1232-ND	FX8C-80P4
	11mm	FX8C-80P-SV6(21)	H1233-ND	

4.5.2 Mating connectors for Bottom/SODIMM side

Mates with	Resulting stacking height	Hirose Part Number	Digikey Order Number	Simple Solutions Order Number
X1301 X1302	9mm	FX8C-100S-SV(21)	H1248-ND	FX8C-100S
	14mm	FX8C-100S-SV5(21)	H1253-ND	
X1303 X1304	9mm	FX8C-80S-SV(21)	H1247-ND	FX8C-80S
	14mm	FX8C-80S-SV5(21)	H1252-ND	

4.6 Oscillators

A maximum of two oscillators can be placed directly on the board. By default only OSC1 is occupied with a 40 MHz oscillator, OSC2 can be occupied by the user.

Various 3.3V standard clock oscillators can be used, for example:

Manufacturer	Part Number	Supplier	Order Number
CTX	CB3LV-3C-40M0000-T	Digikey	CTX280LVCT-ND

Note that 5V TTL oscillators can not be used here.

4.7 JTAG Chain

To allow stacking and mounting in both directions, the JTAG chain is routed as shown in the following diagram:

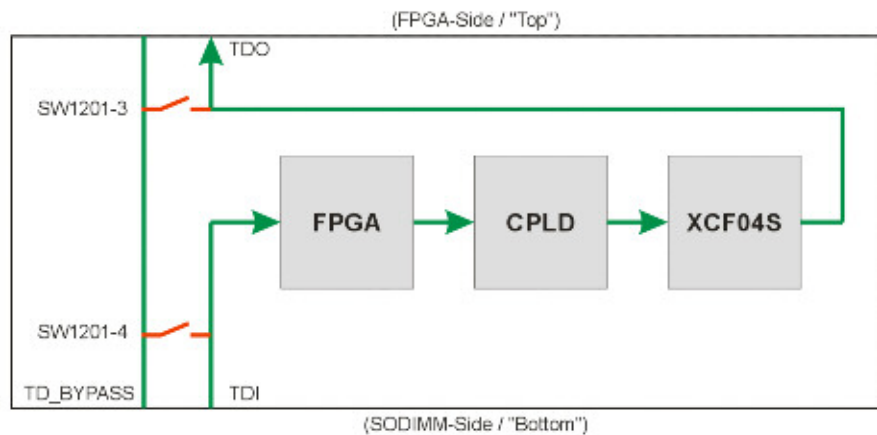


Fig. 4-5

To close the JTAG chain in a system with a single module, one of the switches has to be set depending on which where the JTAG host is connected. In a system with multiple stacked modules, only one switch of one module will be closed. The standard configurations are shown in 4.7.2.

4.7.1 JTAG DIP switch functions

SW1201 Switch Number	Function
3(C)	Connect TDO to BYPASS
4(D)	Connect TDI to BYPASS

Do not close more than one of these two switches at a time, since this would short-circuit the JTAG chain.

4.7.2 Standard JTAG DIP switch settings

For the following examples it is always assumed that JTAG is connected on the baseboard.

4.7.2.1 Single module mounted "Top-Down"

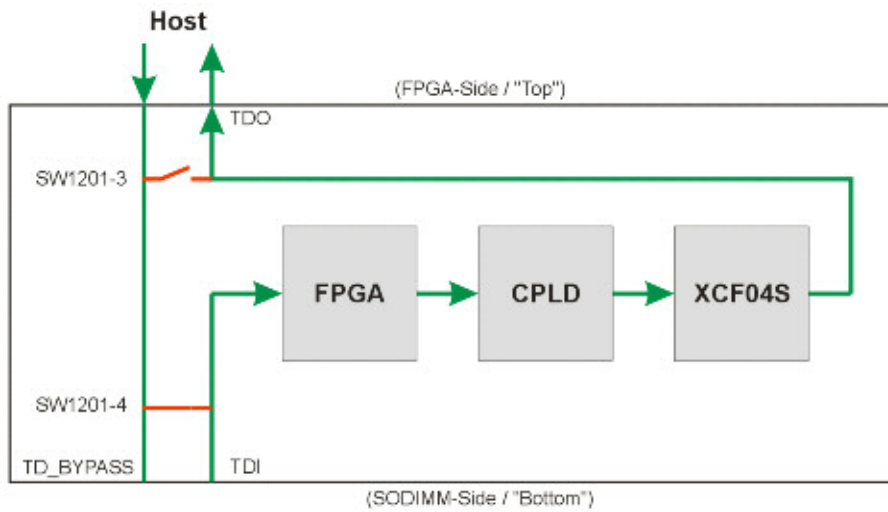


Fig. 4-6

SW1201 Switch Number	Set to
3(C)	0
4(D)	1

4.7.2.2 Single module mounted "Top-Up"

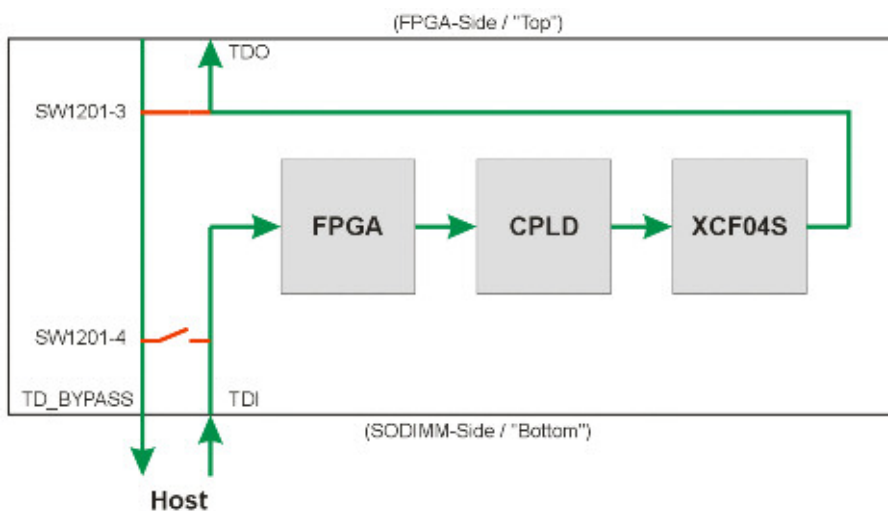


Fig. 4-7

SW1201 Switch Number	Set to
3(C)	1
4(D)	0

4.7.2.3 Stacked modules
("Top-Down" stack shown):

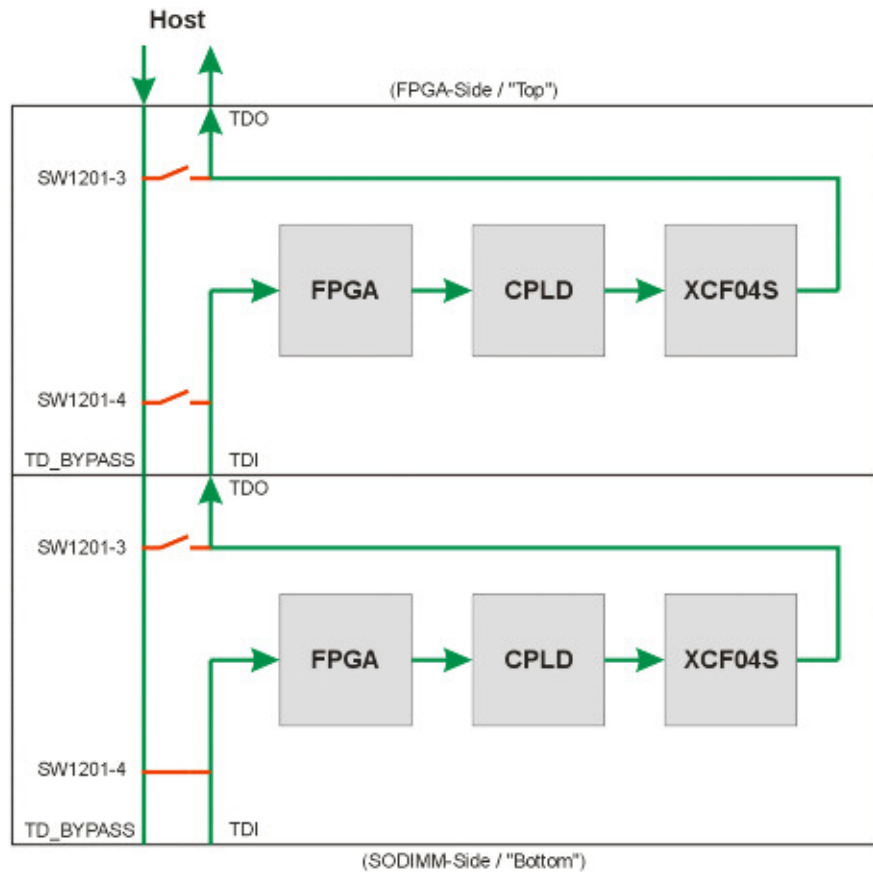


Fig. 4-8

Topmost module of a stack:

SW1201 Switch Number	Set to
3(C)	Same as single module settings
4(D)	

Other modules:

SW1201 Switch Number	Set to
3(C)	0
4(D)	0

This shows, that in a stacked system, mounted top-down, the topmost module will be the first shown in the JTAG chain. In a stacked system mounted bottom-down, the topmost module will be the last shown in the chain.

4.7.3 JTAG on Baseboard

To use the JTAG port of the Baseboard, SB1401 of the Zefant module must be set.

The JTAG-Port on the Baseboard relies on 3,3V being supplied from Zefant Module to Baseboard. Since it is mounted top-down, this is only the case if SB1401 is set!

4.8 Solder bridge configuration

There are 2 solder bridges on the module for power supply configuration:

4.8.1 SB1301

To allow a configurable I/O voltage on banks 2 and 3 of the FPGA, VCCIO of these two banks is connected to pins 41-44 of X1301 (bottom).

If you do not want to supply an I/O voltage yourself, close SB1301 to connect VCCIO of these banks directly to VCC33.

Please remember:

- If the banks are not powered, the Spartan-3 will not run at all!
- If VCCIO is supplied externally, SB1301 has to be open to avoid a short circuit.

SB1301 setting	Function
open	VCCIO2/3 supplied externally on pins 41-44 of X1301 (bottom)
closed	VCCIO2/3 connected to internal 3.3V power supply. This is the default

4.8.2 SB1401

Pins 77-80 of X1302 (bottom) are always connected to VCC33, so they can supply power to external peripherals. This means, that the respective pins of X1402 (top) have to be open, to avoid short-circuiting VCC33 power supplies of neighbour modules.

To allow supplying power to components on top side anyway, SB1401 can be set to connect pins 77-80 of X1402 (top) to VCC33 manually.

If you set this solder bridge, keep in mind to remove it when stacking modules!

SB1401 setting	Function	Standard use
open	X1402 pins 77-80 floating	Stacking of modules
closed	X1402 pins 77-80 connected to VCC33	Powering JTAG or other 3.3V peripherals on top side

5 Signal Descriptions

5.1 Main signal path overview

The main signal paths in the system are shown in the following diagram:

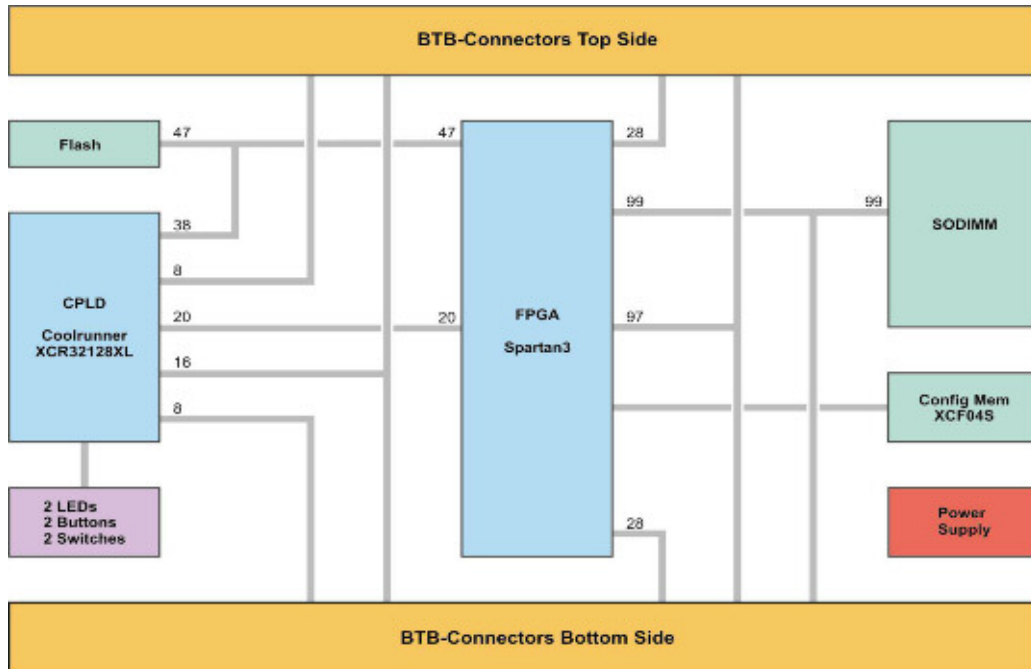


Fig. 5-1

5.2 Signal reference

A signal cross reference between the pins of all active components and connectors is available as an Excel sheet, PDF printout and in basic UCF files on

<http://www.simple-solutions.de/en/support/download/>

Please refer to these resources for complete and most recent informations.

6 Known Issues

6.1 Revision 1.0

- Difficult to press the pushbuttons on the module when it is mounted top-down.
Solved in Rev 1.1: Moved pushbuttons closer to PCB edge.

7 Document Version History

Date	Version	Comments
2005-12-30	V1.6	Added information about board-to-board connectors and oscillators
2005-08-15	V1.5	Corrected faulty component designators in Fig. 4-1 and Fig. 4-2
2005-07-29	V1.4	Added Hole diameter info for mounting holes
2005-07-27	V1.3	Clarified pin numbering of BTB connectors and position of solder bridges
2005-05-18	V1.2	Removed signal cross reference due to redundancy. Please refer to the resources mentioned in ch. 5.2 instead.
2005-05-12	V1.1	Added Mechanical Dimensions, added Contents, Corrected FPGA_IO_DOWN[16..27] in Signal Reference
2005-03-15	V1.0	Initial Release